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EXAMINER	
YU, JAE UN	

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2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/624,421	NGUYEN, VAN D.	
	Examiner	Art Unit	
	Jae U. Yu	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,16,17,19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14, 16, 17 and 19-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The examiner acknowledges the applicant's submission of the RCE dated 5/21/2007. At this point claims 1, 13 and 17 have been amended and claims 15 and 18 have been cancelled. Thus, claims 1-14, 16, 17 and 19-20 are pending in the instant application.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. **Claims 11-14, 16, 17, 19 and 20** are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 11-20 of copending Application No. 11436803. Although the conflicting claims are not identical, they are not patentably distinct from each other because the copending

application has the same scope and teaches every limitation of **claims 12, 14, 16 and 19** from the instant application.

As per **claims 11, 13, 17 and 20**, the copending application has the same scope as the instant application except; that the copending application does not disclose expressly that the "select signal" is actually the "chip select signal" from the instant application and "a controller circuit".

The specification expressly teaches that the "select signal" is in fact a "chip select signal" in paragraph 31.

The specification expressly teaches the "controller circuit" in paragraph 30.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the instant application by including the "chip select signal" and "controller circuit" as taught by the specification in paragraphs 30 and 31. The motivation for doing so would have been logical to physical addressing optimization and the fast operation speed of a hardware circuitry.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-3 and 5-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Borkenhagen et al. (US 5,067,105).

2. **Independent claim 1** discloses, "receiving a command comprising a first logical address **[Receiving a logical card address, Column 3, Lines 60-64]** from the range of logical addresses **[Logical Memory Addresses, Column 3, Lines 60-64]**".

"accessing a look-up table having logical addresses with their corresponding physical addresses **[data structure comprising logical cards and physical cards, Figure 2, Borkenhagen et al.]** from one of the plurality of physical address to find a first physical address, from a range of physical addresses, that corresponds to the first logical address **[Determining a physical card address that corresponds to the logical card address, Figure 2, (Column 3, Line 65 – Column 4, Line 10)]**"

"Generating a chip select signal in response to the first physical address **[Selecting a physical card based on the physical card address, (Column 3, Line 65 – Column 4, Line 10), Figure 1)]** wherein the plurality of ranges of physical addresses include non-contiguous physical address space **[independent physical storage cards, Figure 2]**"

3. **Claim 2** discloses, "the range of physical addresses is contiguous **["physical memory addresses" sharing the same "physical card address", (Column 3, Line 65 – Column 4, Line 10), Figure 1)]**".

4. **Claim 3** discloses, "the range of physical addresses is substantially equivalent to the range of logical addresses **[The "logical memory address" and the corresponding "physical memory address" are identical except the first 3-bits (The identical addresses are materialized in a different physical memory card), (Column 3, Line 60 – Column 4, Line 10)]**".

5. **Claim 5** discloses, "the range of logical addresses are contiguous and the corresponding range of physical addresses is non-contiguous and comprised of a plurality of physical sub-ranges **["physical memory addresses materialized in a plurality of physical memory cards, Figure 2]**".

6. **Claim 6** discloses, "a chip select signal **[Selecting a physical card based on the physical card address, (Column 3, Line 65 – Column 4, Line 10), Figure 1)]** is generated for each physical address sub-range **["physical memory addresses materialized in a plurality of physical memory cards, Figure 2]**".

7. **Claim 7** discloses, "receiving a command comprising a first logical address **[Receiving a logical card address, Column 3, Lines 60-64]** from the range of logical addresses **[Logical Memory Addresses, Column 3, Lines 60-64]**".

"accessing a look-up table having logical addresses with their corresponding physical addresses **[data structure comprising logical cards and physical cards, Figure 2, Borkenhagen et al.]** from one of ranges of physical addresses to find a first physical address, from a range of non-contiguous physical addresses **["physical memory addresses materialized in a plurality of physical memory cards, Figure 2]**, that corresponds to the first logical address **[Determining a physical card address that corresponds to the logical card address, Figure 2, (Column 3, Line 65 – Column 4, Line 10)]**"

"Generating a chip select signal in response to the first physical address **[Selecting a physical card based on the physical card address, (Column 3, Line 65 – Column 4, Line 10), Figure 1)]**"

8. **Claim 8** discloses, "a controller circuit executing an application in which the first logical address is read from memory **[CPU executing an application and generating a logical memory address, Figure 1, Column 3, Lines 60-68]** along with the command".

9. **Claim 9** discloses, "a device manager receiving the first logical address **[Physical card selector logic receiving the first logical address, Figure 1]** from a controller circuit".

10. **Claim 10** discloses, "the device manager generates the chip select signal **[Physical card selector logic selecting appropriate chip, Figure 1, (Column 3, Line 65 – Column 4, Line 10)]** in response to the first physical address".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 4, 11-14, 16, 17, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borkenhagen et al. (US 5,067,105) in view of Daberko (US 5,787,445).

2. As per **claim 4**, Borkenhagen et al. disclose the method recited in claim 1.

Borkenhagen et al. do not disclose expressly, "flash RAM".

Daberko discloses, "flash RAM" in column 3, at lines 14-16.

Borkenhagen et al. and Daberko are analogous art because they are from the same filed of endeavor of increasing fault tolerance by memory access control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Borkenhagen et al. by including a "flash RAM" as taught by Daberko in column 3, at lines 14-16.

The motivation for doing so would have been increased fault tolerance to power interruption as expressly taught by Daberko in column 3, at lines 23-25.

Therefore, it would have been obvious to combine Daberko with Borkenhagen et al. for the benefit of increased fault tolerance to obtain the invention as specified in claim 4.

3. As per **independent claims 11, 13, 17 and 20**, Borkenhagen et al. discloses, "a controller circuit **[[CPU executing an application and generating a logical memory address, Figure 1, Column 3, Lines 60-68]]** executing an application and receiving a first logical address from the range of logical addresses in response to the execution of the application".

"accessing a look-up table having logical addresses with their corresponding physical addresses **[data structure comprising logical cards and physical cards, Figure 2, Borkenhagen et al.]** from one of the plurality of ranges of physical addresses to find a first physical address, from a range of non-contiguous physical addresses **["physical**

memory addresses materialized in a plurality of physical memory cards, Figure 2], that corresponds to the first logical address **[Determining a physical card address that corresponds to the logical card address, Figure 2, (Column 3, Line 65 – Column 4, Line 10)]**"

"Generating a chip select signal in response to the first physical address **[Selecting a physical card based on the physical card address, (Column 3, Line 65 – Column 4, Line 10), Figure 1)]**"

Borkenhagen et al. do not disclose expressly, "flash RAM".

Daberko discloses, "flash RAM" in column 3, at lines 14-16.

Borkenhagen et al. and Daberko are analogous art because they are from the same filed of endeavor of increasing fault tolerance by memory access control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Borkenhagen et al. by including a "flash RAM" as taught by Daberko in column 3, at lines 14-16.

The motivation for doing so would have been increased fault tolerance to power interruption as expressly taught by Daberko in column 3, at lines 23-25.

Therefore, it would have been obvious to combine Daberko with Borkenhagen et al. for the benefit of increased fault tolerance to obtain the invention as specified in claim 11.

4. **Claim 12** discloses, "the plurality of non-contiguous sub-ranges is substantially equal to a logical address range of a flash memory device **[The "logical memory address" and the corresponding "physical memory address" are identical except the first 3-bits (The identical addresses are materialized in a different physical memory card), (Column 3, Line 60 – Column 4, Line 10)]**".

5. **Claim 14** discloses, "the controller circuit is coupled to the plurality of flash memory through a plurality of address lines **[Figure 3C, Daberko]**".

6. **Claims 16 and 19** disclose, "the controller circuit generates the first physical address in response to adding an address offset to the first logical address **[the difference between the generated physical address and the logical address is the "offset", Figure 1]**".

Arguments Concerning Prior Art Rejections

1st Point of Argument

Regarding independent claim 1, the applicant argues that Borkenhagen fails to teach identifying a physical address based on a logical address. However, Borkenhagen

discloses extracting a physical address based on corresponding logical addresses from column 3, line 65 to column 4, line 10.

Further, the applicant argues that Borkenhagen fails to teach the new limitation, "non-contiguous physical address space". However, Borkenhagen discloses a plurality of independent (non-contiguous) physical cards in Figure 2.

Conclusion

A. Claims No Longer in the Application

Claims 15 and 18 were cancelled.

B. Claims Rejected in the Application

Claims 1-14, 16, 17 and 19-20 have received a third action on the merit and are subject of a third action non-final.

C. Direction of Future Remarks

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jae Un Yu who is normally available from 9:00 A.M. to 5:30 P.M. Monday thru Friday and can be reached at the following telephone number: (571) 272-1133.

If attempts to reach the above noted examiner by telephone are unsuccessful, the Examiner's supervisor, Sanjiv Shah, can be reached at the following telephone number: (571) 272-4098.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

August 4, 2007

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